CLAIMS

What is claimed is:

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1. A fabrication method, comprising the steps of:
   (a.) providing a partially fabricated integrated circuit structure which includes **transistors**;
   (b.) forming an **interlevel dielectric** structure over said transistors, said interlevel dielectric including at least
      (i.) a **lower layer** having a first composition,
      (ii.) a **middle layer** having a second composition which is different from said first composition, and
      (iii.) an **upper layer** having a third composition which is different from said second composition;
   (c.) etching through said upper layer, using a relatively isotropic etch process which is selective to said second composition;
   (d.) etching through said middle and lower layers, using a relatively anisotropic etch process, to expose portions of said transistors; and
   (e.) depositing and patterning a thin-film conductor layer, to interconnect said transistors in a desired pattern.

2. The method of Claim 1, wherein said transistors comprise insulated-gate field-effect transistors.

3. The method of Claim 1, wherein said middle layer consists of silicon nitride, and said etching step (c.) comprises wet etching in hydrofluoric acid.

4. The method of Claim 1, wherein said lower layer comprises a doped silicate glass over an undoped silica layer.

5. The method of Claim 1, wherein said upper layer consists of borophosphosilicate glass.

6. The method of Claim 1, wherein said etching step (c.) comprises wet etching.

7. The method of Claim 1, wherein said etching step (d.) comprises plasma etching.

8. The method of Claim 1, wherein said metal layer comprises an adhesion layer, a conductive diffusion barrier layer atop said adhesion layer, and a conductor layer over said diffusion barrier layer.

9. A fabrication method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure which includes **transistors**;

(b.) forming an **interlevel dielectric** structure over said transistors, said interlevel dielectric including at least

(i.) a **lower layer** consisting predominantly of silicate glass,

(ii.) a **middle layer** consisting predominantly of silicon nitride, and

(iii.) an **upper layer** consisting predominantly of doped silicate glass;

(c.) etching through said upper layer, using a relatively isotropic etch process which is selective to said second composition;

(d.) etching through said middle and lower layers, using a relatively anisotropic etch process, to expose portions of said transistors; and

(e.) depositing and patterning a thin-film conductor layer, to interconnect said transistors in a desired pattern.

10. The method of Claim 9, wherein said transistors comprise insulated-gate field-effect transistors.

11. The method of Claim 9, wherein said middle layer consists of silicon nitride, and said etching step (c.) comprises wet etching in hydrofluoric acid.

12. The method of Claim 9, wherein said lower layer comprises a doped silicate glass over an undoped silica layer.

13. The method of Claim 9, wherein said upper layer consists of borophosphosilicate glass.

14. The method of Claim 9, wherein said etching step (c.) comprises wet etching.

15. The method of Claim 9, wherein said etching step (d.) comprises plasma etching.

16. The method of Claim 9, wherein said metal layer comprises an adhesion layer, a conductive diffusion barrier layer atop said adhesion layer, and a conductor layer over said diffusion barrier layer.

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17. A method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure which includes **transistors**;

(b.) forming an **interlevel dielectric** structure over said transistors, said interlevel dielectric including at least

(i.) a **lower layer** having a first composition,

(ii.) a **middle layer** having a second composition which is different from said first composition, and

(iii.) an **upper layer** having a third composition which is different from said second composition;

(c.) etching through said upper layer, using a wet etch process which is selective to said second composition;

(d.) etching through said middle and lower layers, using a relatively anisotropic plasma etch process, to expose portions of said transistors; and

(e.) depositing and patterning a thin-film conductor layer, to interconnect said transistors in a desired pattern.

18. The method of Claim 17, wherein said transistors comprise insulated-gate field-effect transistors.

19. The method of Claim 17, wherein said middle layer consists of silicon nitride, and said etching step (c.) comprises wet etching in hydrofluoric acid.

20. The method of Claim 17, wherein said lower layer comprises a doped silicate glass over an undoped silica layer.

21. The method of Claim 17, wherein said upper layer consists of borophosphosilicate glass.

22. The method of Claim 17, wherein said metal layer comprises an adhesion layer, a conductive diffusion barrier layer atop said adhesion layer, and a conductor layer over said diffusion barrier layer.

23. A method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure which includes **transistors**;

(b.) forming an **interlevel dielectric** structure over said transistors, said interlevel dielectric including at least

(i.) a **lower layer** having a first composition,

(ii.) a **middle layer** having a second composition which is different from said first composition, and

(iii.) an **upper layer** having a third composition which is different from said second composition;

(c.) etching through said upper layer, using a wet etch process which is selective to said second composition;

(d.) etching through said middle and lower layers, using a relatively anisotropic plasma etch process, to expose portions of said transistors; and

(e.) depositing and patterning a thin-film metal layer, without any intermediate etchback steps, to interconnect said transistors in a desired pattern.

24. The method of Claim 23, wherein said transistors comprise insulated-gate field-effect transistors.

25. The method of Claim 23, wherein said middle layer consists of silicon nitride, and said etching step (c.) comprises wet etching in hydrofluoric acid.

26. The method of Claim 23, wherein said lower layer comprises a doped silicate glass over an undoped silica layer.

27. The method of Claim 23, wherein said upper layer consists of borophosphosilicate glass.

28. The method of Claim 23, wherein said etching step (c.) comprises wet etching.

29. The method of Claim 23, wherein said etching step (d.) comprises plasma etching.

30. The method of Claim 23, wherein said metal layer comprises an adhesion layer, a conductive diffusion barrier layer atop said adhesion layer, and a conductor layer over said diffusion barrier layer.

31. An integrated circuit, comprising:

a **substrate** having **transistors** formed at one surface thereof;

an **interlevel dielectric**

overlying said transistors, and

having at least upper, middle, and lower layers, said middle layer having a different composition from said upper layer and from said lower layer, and

having contact holes therein extending vertically therethrough, said contact holes having vertical sidewalls in said lower layer and sloped sidewalls in said upper layer; and

a patterned thin-film **metal layer** extending through said contact holes to interconnect said transistors in a desired electrical configuration.

32. The integrated circuit of Claim 31, wherein said first and third materials both comprise silicate glasses.

33. The integrated circuit of Claim 31, wherein said transistors comprise insulated-gate field-effect transistors.

34. The integrated circuit of Claim 31, wherein said metal layer comprises an adhesion layer, a conductive diffusion barrier layer atop said adhesion layer, and a conductor layer over said diffusion barrier layer.

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